

REMARKS

The specification has been amended to correct some grammatical informalities, which are not related to a reason for patentability. Claims 1-4 remain for consideration in this application.

The disclosure is objected to because of the informalities noted in the Office Action.

Accordingly, the specification has been amended in order to correct the noted informalities. Accordingly, it is submitted that the disclosure has been corrected.

Claims 1-4 are rejected under 35 U.S.C. §103(a) as being unpatentable over the admitted prior (APA) in view of Sakamoto (U.S. Patent No. 5,642,252).

It is the position of the Office Action that Sakamoto discloses the output state detecting means not shown in APA. Additionally, the Office Action indicates that it is inherent that the stopping of supplying the pulse width modulation control signal to the semiconductor element is inherent because the control signal in a closed loop control is an error signal between the output and the desired value. If both values are the same, the error signal will be zero. The Examiner cites Fig. 1.8 in "Modern Control Systems" Bishop, Dorf 7th edition to show this feature. However, the Examiner does not cite this article against the claims.

Sakamoto, as illustrated in Fig. 27 (see also column 17, lines 35-47) discloses a microcomputer having an output into a gate current detecting circuit where the signal is further directed into a power MOSFET with built-in protection circuit. Furthermore, in Sakamoto, the gate current detecting circuit provides an input to the microcomputer which is representative of the state of the gate of the MOSFET.

On the contrary, in claim 1, the “output state detecting means” detects the abnormality of the “output of the semiconductor device” during an overheating operation. Detecting the “output” of the semiconductor device means detecting the state of the source S. Sakamoto detects the state of the gate itself. Thus, this is a distinction between the recitation of claim 1 and the Sakamoto reference.

Furthermore, as noted above, the Office Action states that it is inherent that the pulse width modulation control signal would be stopped. (See page 3 of the Office Action lines 1-10.) It is not clear how the feedback system of Fig. 1.8 in the Bishop, Dorf article states this inherency.

In fact, if the Bishop, Dorf article discloses pertinent features of the claimed invention, then it should be applied as a reference against the claims. It has not. Thus, it is submitted, for the reasons set forth above, that claims 1-4 are not obvious over APA in view of Sakamoto.

In view of the Remarks and amendments set forth above, applicant submits that the Examiner’s objections and rejections have been overcome. Accordingly, it is respectfully requested that the Examiner withdraw the objections and rejection and allow the present claims 1-4.

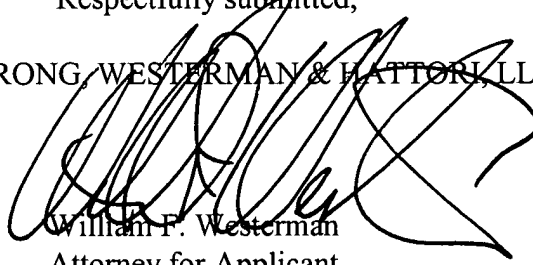
Attached hereto is a marked-up version of the changes made to the specification by the current amendment. The attached page is captioned "**Version with markings to show changes made.**"

U.S. Patent Application Serial No. 09/730,588

In the event that this paper is not timely filed, Applicant respectfully petitions for an appropriate extension of time. Please charge any fees for such an extension of time and any other fees which may be due with respect to this paper, to Deposit Account No. 01-2340.

Respectfully submitted,

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Enclosures: Version with markings to show changes made

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VERSION WITH MARKINGS TO SHOW CHANGES MADE 09/230,588

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IN THE SPECIFICATION:

Please amend the specification as indicated:

Replace the paragraph on page 2, starting with line 18 with the following:

On the other hand, when an abnormality such as the short of the load 4 [arise] arises a large current flows between the source and the drain of the MOSFET 33 due to the PWM control signal coming after that occurrence in the first place, whereby temperature of the [tip] chip rises. The rise in temperature of the chip is detected by the temperature detecting circuit 35, and the detection output is supplied to the latch circuit 36. Subsequently, the output of the latch circuit 36 is supplied to the gate breaking circuit 37. The gate breaking circuit 37 is controlled by the output of the latch circuit 36 so as to protectively intercept a gate input of the MOSFET 33.

Replace the paragraph on page 6, starting with line 9 with the following:

And, in the control circuit of FIG. 1, the output voltage, namely the source voltage, of the MOSFET 33 is detected by the outputting state detecting portion 5 at every fixed monitoring timing, i.e., $T_{g(on)}$ (i.e. the start time of the gate voltage of the MOSFET 33) + T_s (i.e. fixed time period), and the microcomputer 1 judges whether or not the overheat protecting function is operating, based on whether the output state is in high level (HI) or in low level (LO).